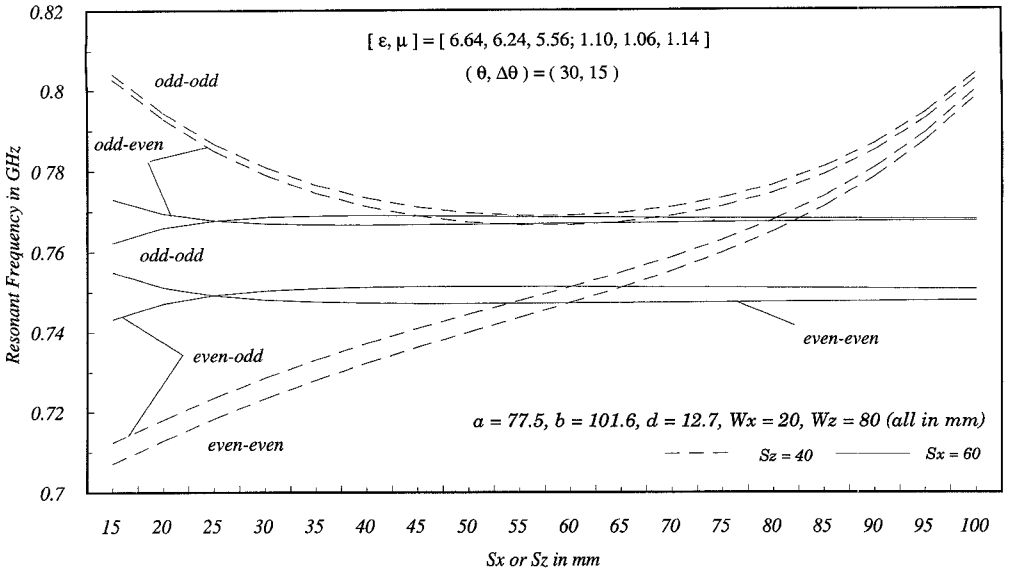

Fig. 4. f_r of all modes of a patch resonator as a function of s_z (solid lines) and s_x (broken lines).

even and even-odd modes. Also in this region, they exhibit totally contrasting behavior—namely, f_rs of o-e and o-o modes decrease, while those of e-e and e-o steadily increase. As the transverse separation between the patches increases, resonant frequencies of the array are significantly influenced by the sidewalls of the waveguide. They all tend to increase towards the same value.

V. Conclusion

Resonant properties of a four microstrip patch resonator array, printed on an anisotropic substrate, were analyzed. Good agreement with limited published data was found, and ample numerical results for resonant frequencies of the resonator array were presented as functions on the geometrical and substrate material parameters.

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A Technique for Minimizing Intermodulation Distortion of GaAs FET's

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***Abstract*—This paper describes the theory to minimize the intermodulation distortion under certain current bias condition for GaAs FET's. A device-parametric study has been done to obtain the general equation that provides the lowest distortion condition as a function of an operating current. Based on the present theory, FET parameters have been designed practically.**

I. Introduction

In recent years, the microwave GaAs MESFET has been widely used for a variety of mobile communication systems. In those portable systems, what is most important is to reduce the operating current since the battery running time is a major concern. In addition, recent digital communication systems require the minimization of an intermodulation (IM) distortion in order to improve the error rate. However, it is difficult that GaAs FET's provide the low current and the low distortion characteristic at the same time. Therefore, the goal

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to design such devices is to determine the device parameter that gives the best IM characteristics under allowed current condition.

Many researchers have attempted to describe the distortion characteristics of GaAs FET's by using the harmonic balance technique with new models of nonlinearities in GaAs FET's or by analyzing nonlinear distortion in GaAs FET's [1]–[5]. Generally, the lowest IM distortion is discussed as a parameter of the operating current for a particular FET. However, the general relation between the operating current and the IM distortion as parameters of the gate bias and gate width has not been clarified. To design the optimum device is to determine these parameters at the same time. In this work, we show the general equation providing the relation between the lowest IM distortion and the operating current as a function of the gate bias and the gate width for the FET amplifier. Based on this general equation, we can design the gate width that offers the lowest IM distortion under the target current condition. It is noted that this theory provides the essential optimum condition. Therefore, this general equation about the IM distortion becomes a practical technique for circuit design. In this paper, this new technique is experimentally applied to the design of a GaAs FET amplifier.

II. General Expression of the IM Distortion

In this section, the general equation that provides the lowest IM distortion under the allowed operating current is obtained. First, the output power and the IM distortion characteristic of the FET are described as a function of the gate width. Then, this distortion characteristic is defined as a parameter of the gate bias. Finally, the condition that provides the best IM distortion at the allowed operating current is obtained.

The output power for the FET with the unit gate width W_g is defined as P_{OUT}. Then, the total output power $P_{\mathrm{OUT}n}$ for the FET that has an n-times as large as the unit gate width ($W_{gn} = n * W_g$), is obtained as follows,

$$\begin{aligned} P_{\mathrm{OUT}n} &= n \cdot \mathrm{Ga} \cdot \frac{P_{\mathrm{IN}}}{n} \\ &= n \cdot \frac{P_{\mathrm{OUT}}}{n} \\ &= P_{\mathrm{OUT}}\ , \end{aligned} \tag{1}$$

where Ga and P_{IN} are the small-signal power gain and the input power of the unit gate width FET, respectively. As the input power is constant, the power injected to each unit gate width FET is divided by n. As a result, $P_{\mathrm{OUT}n}$ is equal to P_{OUT}. In (1), we assume that FET's are small enough so distributed phase effects due to multiple gates can be ignored. Therefore, Ga is not a function of the gate width, and the gate width factor, n, is only for paralleling multiple gates.

On the other hand, as the third-order intermodulation distortion (IM_3) is proportional to P_{IN}^3, the IM_3 for the FET with the gate width W_{gn}, IM_{3n}, is

$$\begin{aligned} \mathrm{IM}_{3n} &= n \cdot \frac{\mathrm{IM}_3}{n^3} \\ &= \frac{\mathrm{IM}_3}{n^2}, \end{aligned}$$

or

$$\mathrm{IM}_{3n}\,[\mathrm{dB}] = \mathrm{IM}_3[\mathrm{dB}] - 20 \cdot \log n. \tag{2}$$

When the gate width of the FET increases n-times, the IM_3 increases only $1/n^2$ in comparison with one of the unit gate width FET.

In general, the third-order intercept point (IP_3) is used in normalizing the distortion performance of devices for comparison. It is defined as the output power at which the intermodulation distortion component equals the fundamental frequency output, when both are extrapolated linearly (on log scales) from low signal levels. Then the IP_3 of the FET with unit gate width is given by

$$\mathrm{IP}_3[\mathrm{dB}] = P_{\mathrm{OUT}}[\mathrm{dB}] + \frac{P_{\mathrm{OUT}}[\mathrm{dB}] - \mathrm{IM}_3[\mathrm{dB}]}{2}. \tag{3}$$

Using (1)–(3), the IP_3 of the total FET with the gate width W_{gn}, IP_{3n}, is obtained as follows,

$$\begin{aligned} \mathrm{IP}_{3n}[\mathrm{dB}] &= P_{\mathrm{OUT}}[\mathrm{dB}] + \frac{P_{\mathrm{OUT}}[\mathrm{dB}] - (\mathrm{IM}_3[\mathrm{dB}] - 20 \cdot \log n)}{2} \\ &= \mathrm{IP}_3[\mathrm{dB}] + 10 \cdot \log n. \end{aligned} \tag{4}$$

or

$$\mathrm{IP}_{3n} = n \cdot \mathrm{IP}_3. \tag{5}$$

Also, the IP_3 is changed by the operating current. Then, we lead the equation by which the maximum IP_3 is obtained to describe IP_3 as a function of the operating current. For the unit gate width FET, the IP_3 is defined as

$$\mathrm{IP}_3 = f(i_{\mathrm{ds}}), \tag{6}$$

where i_{ds} is the operating current of the unit gate width FET. In this case, i_{ds} is changed by the gate bias voltage V_{gs}. Therefore, the symbol of "i_{ds}" means the gate bias condition. Combining (6) with (5), the IP_3 of the FET with the gate width W_{gn}, IP_{3n}, is

$$\mathrm{IP}_{3n} = n \cdot f(i_{\mathrm{ds}}). \tag{7}$$

Now, when the operating current of the FET with the gate width W_{gn} is defined as I_{ds}, I_{ds} is given as follows by using i_{ds},

$$I_{\mathrm{ds}} = n \cdot i_{\mathrm{ds}}. \tag{8}$$

Therefore, from (7) and (8), the relation of the IP_3 and the operating current of the FET with the gate width W_{gn} is

$$\mathrm{IP}_{3n} = n \cdot f\left(\frac{I_{\mathrm{ds}}}{n}\right). \tag{9}$$

Equation (9) means that IP_3 is changed by two parameters, such as the gate width parameter n and operating current parameter I_{ds}. When the one of these parameters is fixed, the other parameter that maximizes the IP_3 can be designed. In this case, the operating current is fixed. Therefore, this maximum IP_3 condition is described as

$$\frac{\partial}{\partial n}\mathrm{IP}_{3n}\Big|_{I_{\mathrm{ds}}=\mathrm{const}} = 0. \tag{10}$$

Substituting (9) to (10), the condition can be described as follows,

$$\begin{aligned} \frac{\partial}{\partial n}\mathrm{IP}_{3n} &= \frac{\partial i_{\mathrm{ds}}}{\partial n} \cdot \frac{\partial}{\partial i_{\mathrm{ds}}}\mathrm{IP}_{3n} \\ &= -\frac{I_{\mathrm{ds}}}{n^2}\left[\left(-\frac{I_{\mathrm{ds}}}{i_{\mathrm{ds}}^2}\right)f(i_{\mathrm{ds}}) + \frac{I_{\mathrm{ds}}}{i_{\mathrm{ds}}}\frac{\partial}{\partial i_{\mathrm{ds}}}f(i_{\mathrm{ds}})\right] \\ &= 0. \end{aligned}$$

Therefore,

$$f(i_{\mathrm{ds}}) = i_{\mathrm{ds}}\frac{\partial}{\partial i_{\mathrm{ds}}}f(i_{\mathrm{ds}}). \tag{11}$$

The solution of (11) corresponds to the point of tangency of the functional curve $f(i_{\mathrm{ds}})$ and a straight line passing through the origin (0, 0). From (11), the condition of the maximum IP_3 under the allowed operating current is provided. This result shows that the bias condition providing the maximum IP_3 is constant for various gate width FET's. It is noted that for the target operating current, the optimum gate width offering the maximum IP_3 can be designed by

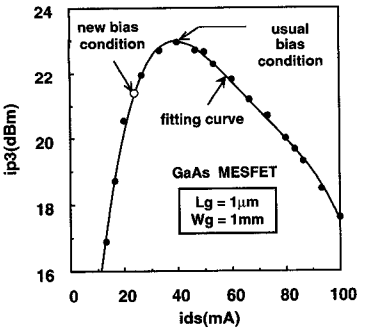

Fig. 1. Measurement result of the function of $f(i_{\rm ds})$.

(11). When the solution of this equation is represented as $i_{\rm ds0}$, the optimum gate width W_{g0} is given as

$$W_{g0} = \frac{I_{\rm ds}}{i_{\rm ds0}} \cdot W_{g0}. \tag{12}$$

Therefore, the general expression of the maximum IP_3 condition is represented as

$$IP_{3\max} = \frac{I_{\rm ds}}{i_{\rm ds0}} \cdot f(i_{\rm ds0}). \tag{13}$$

In this way, to achieve the maximum IP_3 under the allowed operating current, the gate width and the gate bias condition are designed at the same time. The general expression of the IM distortion is represented by (11)–(13). From this theory, we can find that the usual design technique that separately decides the gate width and the gate bias cannot reach the maximum IP_3. It is noted that we can design the condition of the maximum IP_3 for the target operating current, only when the gate width is provided by this general expression.

III. Description of the Function $f(i_{\rm ds})$

In the previous section, it is found that the function $f(i_{\rm ds})$ is required to calculate the condition that maximizes the IP_3 for the allowed operating current. This function means the distortion characteristic of the unit gate width FET as a function of the gate bias condition. It is the objective of this section to describe the function $f(i_{\rm ds})$. For example, we use the measurement result.

Figure 1 shows the measurement result of the relation between $i_{\rm ds}$ and IP_3 for the unit gate width FET. The device used in the experiment is a 1-μm gate-length and -2 V threshold voltage GaAs MESFET. The relation $f(i_{\rm ds})$ is approximated as

$$f(i_{\rm ds}) = a + b \cdot i_{\rm ds} + c \cdot i_{\rm ds}^2 + d \cdot i_{\rm ds}^3 + e \cdot i_{\rm ds}^4. \tag{14}$$

It is convenient to represent $f(i_{\rm ds})$ as a polynomial expression to calculate (11). Fitting the relation of Fig. 1 to (14), each coefficient is shown in Table I. These value is empirically fitted to only one FET. From (11) and (14), the $i_{\rm ds0}$ value is obtained as 24.5 mA. It should be noted that this value is different from the condition that maximizes the IP_3 of the unit gate width FET in Fig. 1. This result shows that we must simultaneously design the bias condition and the gate width to obtain the $IP_{3\max}$ of (13) at the target operating current.

In this paper, we use the measurement result to describe the function $f(i_{\rm ds})$. Another way that describes $f(i_{\rm ds})$ is the use of the nonlinear FET model, such as Curtice cubic model [6], Statz model [7], and so on.

IV. Calculation Result

In this section, the $i_{\rm ds0}$ value that is calculated in the previous section is discussed. It is worthwhile to compare this bias condition with usual one. Usually, the gate bias is set to the condition that maximizes IP_3 for each gate width FET. In Fig. 1, this value is obtained as 40.1 mA. Therefore, it is different from the $i_{\rm ds0}$ value that is calculated in the previous section. Substituting these gate bias conditions to (13) and (14), the relation between $IP_{3\max}$ and $I_{\rm ds}$ as a parameter of the gate width is shown in Fig. 2. The solid line shows the relation with this new technique and the broken line shows that with usual one, respectively. In Fig. 2, the value of IP_3 is increased by 1.2 dB to compare with the use of the usual technique at the Ids of 21 mA. This figure also shows the Ids value that is required to achieve the target IP_3 value. For example, to obtain an IP_3 of 20 dBm, the required $I_{\rm ds}$ is 21 mA for the usual technique. But it is 17 mA for this new one. This result shows that $I_{\rm ds}$ can be decreased by 20%. This new technique, for instance, contributes to the reduction of the consumption power for the machine of the cellular phone.

TABLE I
Coefficient Value of the Fitted Equation

coefficient	fitted value	
a	-2.1 E2	mW
b	2.5 E1	mW / mA
c	5 2 E-1	mW / mA^2
d	4.2 E-3	mW / mA^3
e	1.2 E-5	mW / mA^4

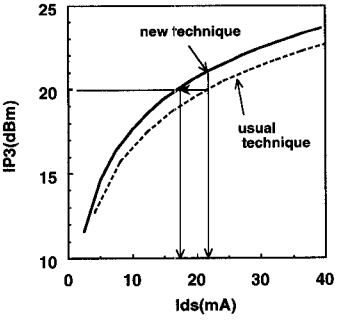

Fig. 2. Calculation results of the relation between $I_{\rm ds}$ and IP_3.

V. Conclusion

A relation between the intermodulation distortion and the operating current as parameters of the gate bias condition and the gate width in microwave MESFET amplifiers has been presented. It shows that we must simultaneously design the gate bias condition and the gate width to achieve the maximum IP_3 for the target $I_{\rm ds}$. Using this new technique, $I_{\rm ds}$ can be reduced by 20% in comparison with the use of the usual one.

Acknowledgment

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LRM Probe-Tip Calibrations using Nonideal Standards

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Abstract—**The line-reflect-match calibration is enhanced to accommodate imperfect match standards and lossy lines typical of monolithic microwave integrated circuits. We characterize the match and line standards using an additional line standard of moderate length. The new method provides a practical means of obtaining accurate, wideband calibrations with compact standard sets. Without the enhancement, calibration errors due to imperfections in typical standards can be severe.**

I. Introduction

This paper, which has been presented in conference [1], shows how line-reflect-match (LRM) calibrations of microwave probe stations can be extended to cases in which the match and line standards are imperfect.

Eul and Schiek [2] introduced LRM as an alternative to the thru-reflect-line (TRL) calibration [3]. They noted that the LRM calibration sets the reference impedance to the impedance of the match standard, which is generally unknown except at dc. This is further discussed in [4].

More recently, Barr and Pervere [5] studied the LRM calibration and noted that a characterization of the lossy line is also necessary in order to translate the reference plane. They did not suggest a means of performing this characterization, however. Davidson, *et al.* [6] applied the LRM technique with the intent of obtaining a probe-tip calibration, that is, a probe-station calibration with reference plane near the probe tips and reference impedance of 50 Ω. As a match standard, these authors used resistors trimmed to a dc resistance of 50 Ω. They attempted to determine the resistor reactance and concluded that it was small. They achieved the reference plane translation by using a very short low-loss line standard, estimating its parameters from lossless approximations. These implementations of the LRM calibration are therefore limited to ideal match standards and to short low-loss line standards.

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In [7], Davidson, *et al.* introduced a procedure which attempts to determine and account for the reactance of the planar resistors they used as match standards. They achieved this by introducing a lossless reflect into the calibration. This method is still limited to match standards with a frequency-independent resistance and with a reactance due only to a frequency-independent inductance, to short low-loss line standards, and to lossless reflects.

The multiline TRL calibration [8] does not suffer from these limitations. Because it is based on the TRL algorithm, it measures the ratios of traveling waves in the transmission lines [4]. The bandwidth and accuracy of the calibration are increased over conventional TRL by the use of multiple lines. The calibration also measures the propagation constant of the line standards so that the calibration reference impedance and the reference plane can be set accurately [9], [10]. The calibration is thus especially well suited to monolithic microwave integrated circuits (MMIC's), in which wide bandwidth is needed and small geometries result in very lossy lines with a complex frequency-dependent characteristic impedance.

The multiline TRL calibration suffers one important drawback, however. To obtain a wide measurement bandwidth, a set of lines, some quite long, is required; this uses expensive space on the wafer. When realized in MMIC form, LRM standards while far more compact than multiline TRL standards, are incompatible with conventional LRM assumptions. Typical imperfections include match standards with process-dependent dc resistance and frequency-dependent resistance and inductance [11], lossy line standards, and lossy reflects, are incompatible with the assumptions of conventional implementations of LRM.

In this paper we show how to modify the LRM calibration to account for the imperfect match and line standards typical of MMIC's. We first study coplanar waveguide (CPW) resistors and lines, evaluating separately their use as match and line standards in LRM probe-tip calibrations. We show that both the real and imaginary parts of the resistor impedance must be known if the LRM reference impedance, which is initially set to the impedance of the match, is to be reset to some standard value (e.g. 50 Ω). We also show that the line loss and characteristic impedance must be considered when setting the reference plane position. Finally, we examine a TRL calibration with a single line moderately longer than the thru line and show that it is accurate enough in practice to characterize the match and line standards. This results in a practical means of obtaining accurate wideband calibrations with a compact standard set consisting of a thru line, a reflect, a match standard, and a second line standard of moderate length.

II. Reference Impedance

For these experiments we constructed a set of CPW calibration artifacts, typical of those found on MMIC's, on a gallium arsenide substrate. The artifacts consisted of a CPW thru line 550 μm long, four longer lines of length 2.685 mm, 3.75 mm, 7.115 mm, and 20.245 mm, and two shorts offset 0.225 mm from the beginning of the line. We also fabricated a match standard by terminating a 275 μm section of the CPW with a single 73 μm by 73 μm nickel-chromium thin-film resistor; the resistor geometry is described in [11]. These artifacts were fabricated with a 0.5 μm evaporated gold film adhered to the 500 μm gallium arsenide substrate with an approximately 50 nm titanium adhesion layer. The lines had a center conductor of width 73 μm separated from two 250 μm ground planes by 49 μm gaps.